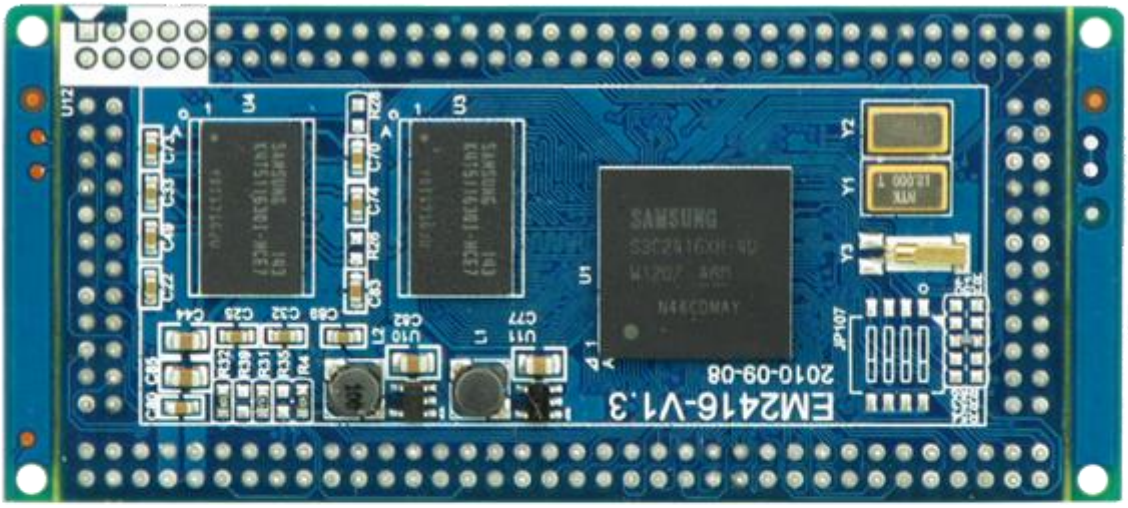
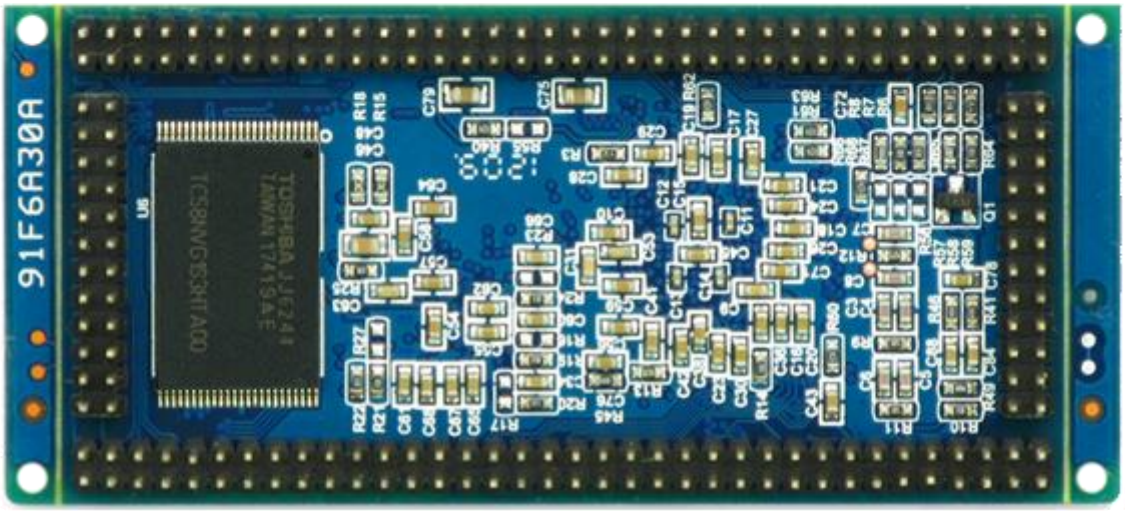
MINI2416-III Module
Reference User Manual





1. Introduction

1.1. About this Manual

This manual is intended to provide the user with an overview of the board and benefits, complete features specifications, and set up procedures. It contains important safety information as well.

1.2. Feedback and Update to this Manual

To help our customers make the most of our products, we are continually making additional and updated resources available on the Boardcon website (www.armdesigner.com).
These include manuals, application notes, programming examples, and updated software and hardware. Check in periodically to see what's new!
When we are prioritizing work on these updated resources, feedback from customers is the number one influence, If you have questions, comments, or concerns about your product or project, please no hesitate to contact us at support@armdesigner.com.

1.3. Limited Warranty

Boardcon warrants this product to be free of defects in material and workmanship for a period of one year from date of buy. During this warranty period Boardcon will repair or replace the defective unit in accordance with the following process:
A copy of the original invoice must be included when returning the defective unit to Boardcon. This limited warranty does not cover damages resulting from lighting or other power surges, misuse, abuse, abnormal conditions of operation, or attempts to alter or modify the function of the product.
This warranty is limited to the repair or replacement of the defective unit .In no event shall Boardcon be liable or responsible for any loss or damages, including but not limited to any lost profits, incidental or consequential damages, loss of business, or anticipatory profits arising from the use or inability to use this products.
Repairs make after the expiration of the warranty period are subject to a repair charge and the cost of return shipping. Please contact Boardcon to arrange for any repair service and to obtain repair charge information.

Content

Chapter 1 About the Module

1.1 Brief introduction

MINI2416-III is System-On-Module (SOM) based on the Sumsung's S3C2416XH-40 RISC microprocessor with ARM 9 core in small size, powerful 2D graphic engine. low-power, and high-performance.
The module has all pins function of S3C2416, low cost and hight performance. Compatible with MINI2440.
Stable electrical performance, Successful mass production. applicable to POS, Slot Machine, and Terminal controller.

1.2 Featrues and Functionality

1.2.1 Software Features

- U-boot 1.3.4
  - Supporting Nand Flash erase/write/read
  - Supporting Nand Flash erase/write/read
  - Supporting set, save Environment Variables
  - Supporting SD Card boot-up(replace JTAG)
  - Supporting bootm, bootargs setting

Warnning: We strongly recommend Hardware ECC for ECC check. As compared with Software ECC, Hardware ECC is more stable and faster, but Software ECC takes up more resources, and its checking ability is not as good as hardware ECC.

- Kernel and drivers
  - Kernel: Linux2.6.21
  - Supporting Serial ports, RTC, LCD, Touch Screen, SD card,
  - Supporting Audio, Nand flash, WIFI, GSM/GPRS, GPS,
  - supporting update image from SD
- File system
  - Yaffs File System, busybox, Provided Lib(ALSA-lib, tslib, glibc), udev support
- Embedded GUI
  - Qtopia2.2.0
- Cross complier Environment
  - Cross-4.2.2-eabi

1.2.2 Hardware Features

- CPU
  - Samsung S3C2416XH, 400MHz, ARM926 Core
- RAM
  - On-board 128MB DDR2-RAM
  - 16bit data bus
  - DDR clock frequency as high as 100MHz
- ROM
  - On-board SLC or MLC 256MB Nand Flash
  - Up to 4GB
- POWER
  - high-efficiency DC-DC converter
  - 3.3V Power input
- RTC
- JTAG
- AUDIO interface
  - Support I2S/AC97/PCM
  - Support 6-ch audio output
- Watchdog
- 1 Pin Fast Boot Mode Set
- 4 UART (2 five line and 2 three line)
- IIC interface
- 1 HS-ISP BUS
  - Supports 8bit/16bit/32bit data full duplex
  - Two independent FIFOs
- SDIO interface
  - 2 4bit SDIO
  - Boot in SDIO CH1
- 10 12bit ADIN or 6 ADIN and 4 wire RES-touch panel interface
- 16 interrupt sources and 24 GPIOs
- 2 USB interface (2.0 Device and 1.1 HOST)
- 4 PWM Timer out
- 2 Clock out
- TFT LCD BUS
  - 24BPP RGB parallel output
  - PIP(OSD) function
- 16 bit ISA BUS

1.3 Key Components

No.	M. S. Code	Spec	Packing	Mark
1	U00006	S3C2416XH-40	FBGA330	

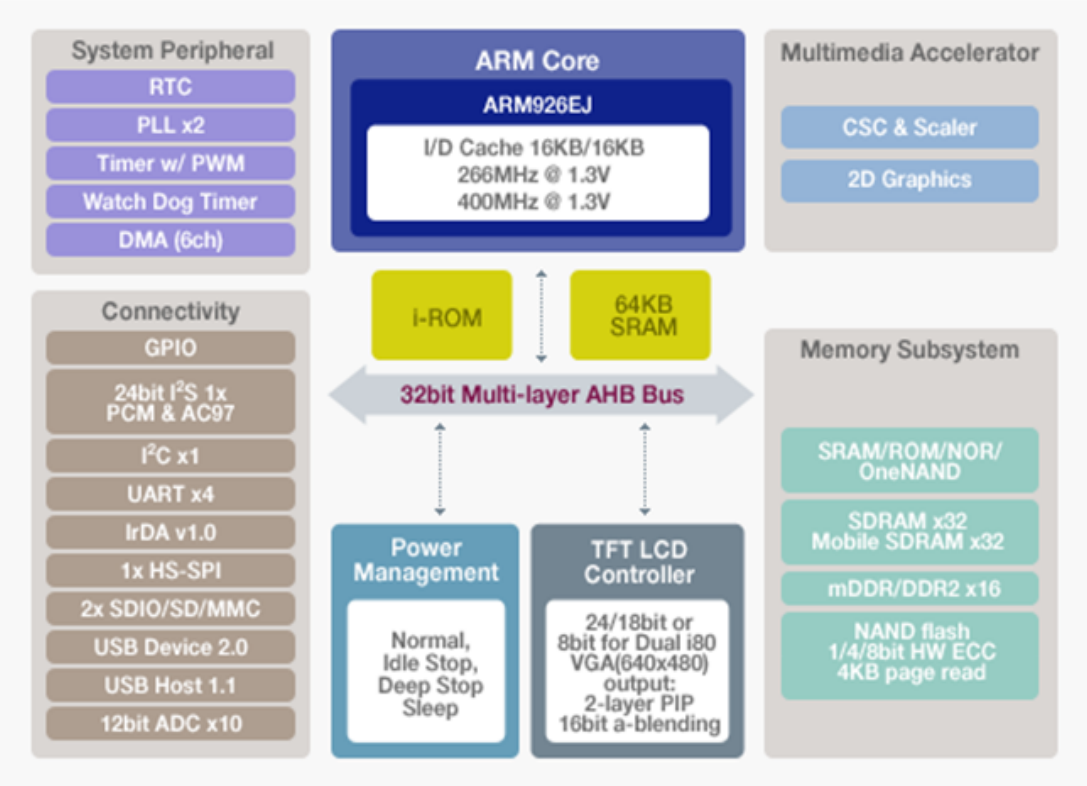
2	U02005	K4T51163QQ-BCE7	FBGA84	
3	U01005	TC58NVG1S3HTA00	TSOP48	
4	J00012	Coreboard/dip	CON192BOTTOM_2.0	
5	J00016			

1.4 Block Diagram

- ***CPU***

S3C2416

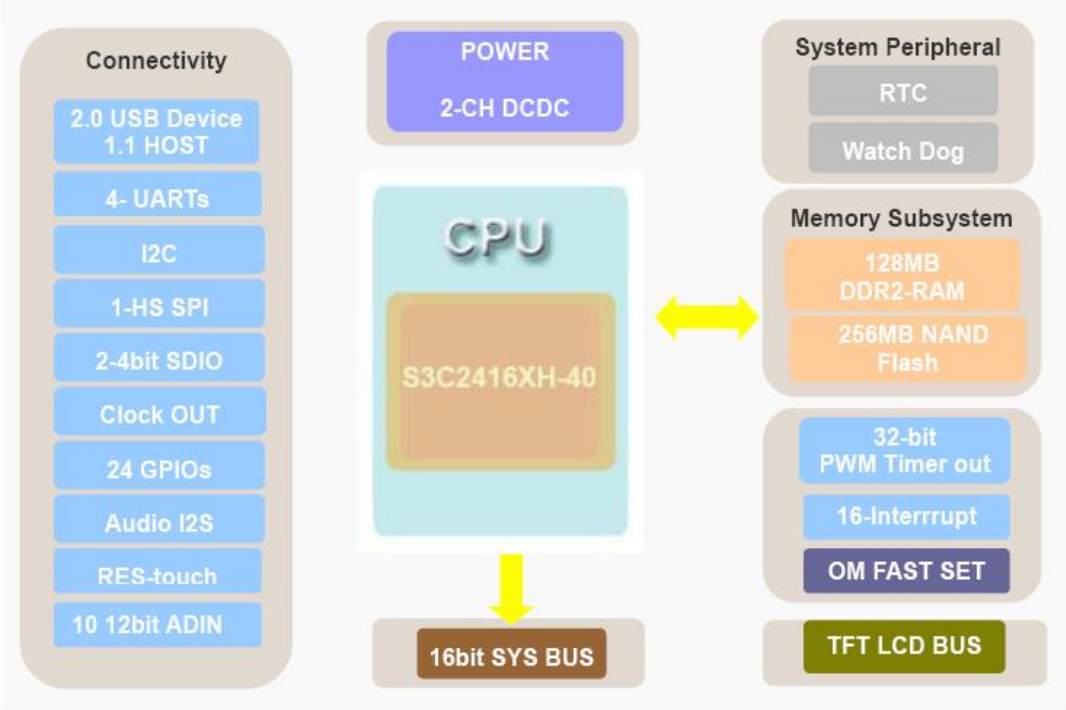
Block Diagram



- ***Module***

MINI2416-III

Block Diagram



1.5 Module Pinout

Pin	Signal name	Function	Description	IO Type
1	DATA6	RDATA6	Flash Data Bus	I/O
2	DATA7	RDATA7	Flash Data Bus	I/O
3	ADDR7	RADDR7	Address Bus	O
4	ADDR8	RADDR8	Address Bus	O
5	ADDR5	RADDR5	Address Bus	O
6	ADDR6	RADDR6	Address Bus	O
7	ADDR3	RADDR3	Address Bus	O
8	ADDR4	RADDR4	Address Bus	O
9	ADDR1	RADDR1	Address Bus	O
10	ADDR2	RADDR2	Address Bus	O
11	SDATA30	GPK14	Only GPIO function	I/O
12	SDATA31	GPK15	Only GPIO function	I/O
13	SDATA28	GPK12	Only GPIO function	I/O
Pin	Signal name	Function	Description	IO Type
14	SDATA29	GPK13	Only GPIO function	I/O
15	SDATA26	GPK10	Only GPIO function	I/O
16	SDATA27	GPK11	Only GPIO function	I/O
17	SDATA24	GPK8	Only GPIO function	I/O
18	SDATA25	GPK9	Only GPIO function	I/O
19	SDATA22	GPK6	Only GPIO function	I/O

20	SDATA23	GPK7	Only GPIO function	I/O
21	SDATA20	GPK4	Only GPIO function	I/O
22	SDATA21	GPK5	Only GPIO function	I/O
23	SDATA18	GPK2	Only GPIO function	I/O
24	SDATA19	GPK3	Only GPIO function	I/O
25	SDATA16	GPK0	Only GPIO function	I/O
26	SDATA17	GPK1	Only GPIO function	I/O
27	TRSTn	nTRST	Reset the TAP controller at start	I
28	nRESET	nRESET	Reset the system	I
29	TDO	TDO	TAP controller data output	O
30	TDI	TDI	TAP controller data input	I
31	TCK	TCK	TAP controller clock	I
32	TMS	TMS	TAP controller mode select	I
33	RXD2	UART RXD CH2	Uart receives data input	I
34	TXD2	UART TXD CH2	Uart transmits data output	O
35	RXD1	UART RXD CH1	Uart receives data input	I
36	TXD1	UART TXD CH1	Uart transmits data output	O
37	RXD0	UART RXD CH0	Uart receives data input	I
38	TXD0	UART TXD CH0	Uart transmits data output	O
39	RTSn0	UART RTS CH0	Uart request to send output signal	O
40	CTSn0	UART CTS CH0	Uart clear to send input signal	I
41	RTSn1	UART RTS CH1	Uart request to send output signal	O
42	CTSn1	UART CTS CH1	Uart clear to send input signal	I
43	RXD3	UART RXD CH3	Uart receives data input	I
44	TXD3	UART TXD CH3	Uart transmits data output	O
45	IRQ_LAN	EINT4/GPF4	Used for DM9000 IRQ	I/O
46	EINT5	EINT5/GPF5		I/O
47	EINT6	EINT6/GPF6		I/O
48	EINT7	EINT7/GPF7		I/O
49	EINT8	EINT8/GPF8		I/O
50	EINT11	EINT11/GPF11		I/O
51	EINT14	EINT14/GPF14		I/O
52	EINT13	EINT13/GPF13		I/O
53	EINT15	EINT15/GPF15		I/O
Pin	Signal name	Function	Description	IO Type
54	EINT12	EINT12/GPF12		I/O
55	EINT10	EINT10/GPF10		I/O
56	EINT9	EINT9/GPF9		I/O
57	VBUS_DET	EINT2/GPF2	Used for USB device	I/O
58	VDD_RTC	RTC battery in	3.6V ~ 2.5V	P
59	DP_UDEV	DP_UDEV	DATA(+) for USB Device	I/O
60	ADCIN3	ADC IN3	0.1 uF CAP pull down & close to module	I

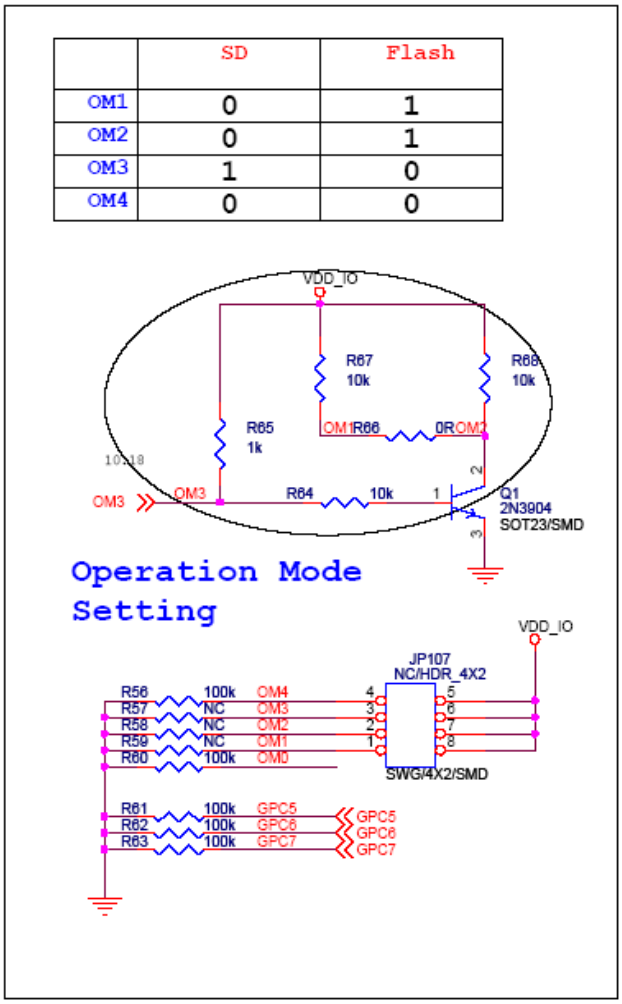
61	DM_UDEV	DM_UDEV	DATA(-) for USB Device	I/O
62	ADCIN2	ADC IN2	0.1 uF CAP pull down & close to module	I
63	USBDN	USB Host DN	Need to 15K resistor pull down	I/O
64	ADCIN1	ADC IN1	0.1 uF CAP pull down & close to module	I
65	USBDP	USB Host DN	Need to 15K resitstor pull down	I/O
66	ADCIN0	ADC IN0	0.1 uF CAP pull down & close to module	I
67	SPIMISO	SPIMISO/GPE11	SPI master data in or slave data out	I/O
68	SPICS	SPICS/GPL13	SPI chip select for slave mode	I/O
69	SPICLK	SPICLK/GPE13	SPI clock output	I/O
70	SPIMOSI	SPIMOSI/GPE12	SPI master data out or slave data in	I/O
71	EINT0	EINT9/GPF9		I/O
72	GPB6	nXBREQ/GPB6	Bus Hold Request	I/O
73	CLKOUT1	CLKOUT1/GPH14	Clock output signal	I/O
74	GPC0	GPC0/RGB_LEND	RGB I/F line end or i80 I/F out enable	I/O
75	NC	NC/RADDR21	Address Bus	O
76	NC	NC/RADDR22	Address Bus	O
77	OM3	OM_SET/RADDR23	OM Fast Set Pin or Address Bus	I/O
78	NC	NC/RADDR24	Address Bus	O
79	SD1_CDn	EINT3/GPF3	Used for SD1 card CDn	I/O
80	SD1_DAT2	SD1_DAT2/GPL2	SD1 data	I/O
81	SD1_DAT3	SD1_DAT3/GPL3	SD1 data	I/O
82	SD1_CMD	SD1_CMD/GPL8	Receive response/transmit command	I/O
83	SD1_CLK	SD1_CLK/GPL9	SD1 clock	O
84	SD1_DAT0	SD1_DAT0/GPL0	SD1 data	I/O
85	SD1_DAT1	SD1_DAT1/GPE8	SD1 data	I/O
86	SD1_WPn	GPB4/TCLK	External timer clock input	I/O
87	GPA23	RSMCLK/GPA23	SMC Clock	I/O
88	I2S_CDCLK	I2S_CDCLK/GPE2	Codec system clock	I/O
89	I2S_LRCK	I2S_LRCK/GPE0	I2S bus channel select clock	I/O
90	I2S_SCLK	I2S_SCLK/GPE1	I2S bus serial clock	I/O
91	GPA24	RSMVAD/GPA24	SMC Address Valid	I/O
92	GPM0	RSMBWAIT/GPM0	SMC Burst Wait	I/O
93	I2S_SDI	I2S_SDI/GPE3	I2S bus serial data input	I/O
Pin	Signal name	Function	Description	IO Type
94	I2S_SDO	I2S_SDO/GPE4	I2S bus serial data output	I/O
95	LCD_PWEN	nXBACK/GPB5	Bus hold acknowledge	I/O
96	TSXP	TSXP/ADC IN9	1 nF cap pull down and close to module	I
97	TSXM	TSXP/ADC IN8	1 nF cap pull down and close to module	I
98	TSYP	TSYP/ADC IN7	1 nF cap pull down and close to module	I
99	TSYM	TSYM/ADC IN6	1 nF cap pull down and close to module	I
100	VCLK	RGB_VCLK/GPC1	LCD Clock or GPC1	I/O
101	HSYNC	RGB_HS/GPC2	RGB Horizontal sync or GPC2	I/O

102	VSYNC	RGB_VS/GPC3	RGB Vertival sync or GPC3	I/O
103	VDEN	RGB_VDEN/GPC4	RGB Data Enable or GPC4	I/O
104	I2C_SCL	I2C_SCL/GPE14	I2C bus clock	I/O
105	I2C_SDA	I2C_SDA/GPE15	I2C bus data	I/O
106	VD23	RGB_DATA23/GPD15	RGB Data23 or GPD15	I/O
107	VD22	RGB_DATA22/GPD14	RGB Data22 or GPD14	I/O
108	VD21	RGB_DATA21/GPD13	RGB Data21 or GPD13	I/O
109	VD20	RGB_DATA20/GPD12	RGB Data20 or GPD12	I/O
110	VD19	RGB_DATA19/GPD11	RGB Data19 or GPD11	I/O
111	VD18	RGB_DATA18/GPD10	RGB Data18 or GPD10	I/O
112	VD17	RGB_DATA17/GPD9	RGB Data17 or GPD9	I/O
113	VD16	RGB_DATA16/GPD8	RGB Data16 or GPD8	I/O
114	VD15	RGB_DATA15/GPD7	RGB Data15 or GPD7	I/O
115	VD14	RGB_DATA14/GPD6	RGB Data14 or GPD6	I/O
116	VD13	RGB_DATA13/GPD5	RGB Data13 or GPD5	I/O
117	VD12	RGB_DATA12/GPD4	RGB Data12 or GPD4	I/O
118	VD11	RGB_DATA11/GPD3	RGB Data11 or GPD3	I/O
119	VD10	RGB_DATA10/GPD2	RGB Data10 or GPD2	I/O
120	VD9	RGB_DATA9/GPD1	RGB Data9 or GPD1	I/O
121	VD8	RGB_DATA8/GPD0	RGB Data8 or GPD0	I/O
122	VD7	RGB_DATA7/GPC15	RGB Data7 or GPC15	I/O
123	VD6	RGB_DATA6/GPC14	RGB Data6 or GPC14	I/O
124	VD5	RGB_DATA5/GPC13	RGB Data5 or GPC13	I/O
125	VD4	RGB_DATA4/GPC12	RGB Data4 or GPC12	I/O
126	VD3	RGB_DATA3/GPC11	RGB Data3 or GPC11	I/O
127	VD2	RGB_DATA2/GPC10	RGB Data2 or GPC10	I/O
128	VD1	RGB_DATA1/GPC9	RGB Data1 or GPC9	I/O
129	VD0	RGB_DATA0/GPC8	RGB Data0 or GPC8	I/O
130	GPB9	nXDACK0/I2S_SDO1	External DMA acknowledge	I/O
131	GPB10	nXDREQ0/I2S_SDO2	External DMA request	I/O
132	ADCIN4	ADC IN4	0.1 uF CAP pull down & close to module	I
133	ADCIN5	ADC IN5	0.1 uF CAP pull down & close to module	I
Pin	Signal name	Function	Description	IO Type
134	TOUT3	TOUT3/GPB3	PWM Timer output	O
135	TOUT2	TOUT2/GPB2	PWM Timer output	O
136	TOUT1	TOUT1/GPB1	PWM Timer output	O
137	TOUT0	TOUT0/GPB0	PWM Timer output	O
138	GPA21	nRSTOUT/GPA21	For extemal device reset control	O
139	nBATF	nBATT_FLT	Probe for battery state	I
140	BEn0	nRBE0	Upper byte/lower byte enable for SDR	O
141	BEn1	nRBE1	Upper byte/lower byte enable for SDR	O
142	CLKOUT0	CLKOUT0/GPH13		I/O

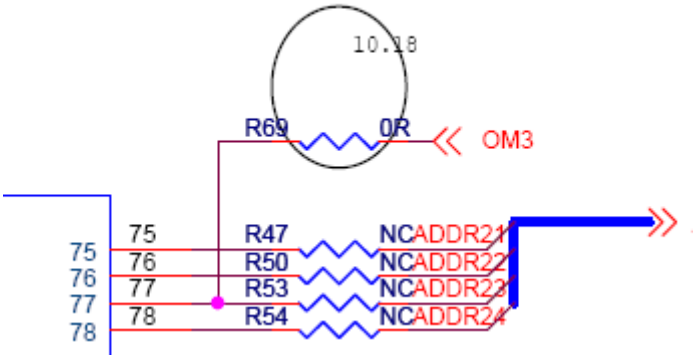
143	SD0_CDn	EINT1/GPF1	Use for SD0 CDn	I
144	SD0_DAT2	SD0_DAT2/GPE7	SD0 data	I/O
145	SD0_DAT3	SD0_DAT3/GPE10	SD0 data	I/O
146	SD0_CMD	SD0_CMD/GPE6	Receive response/transmit command	I/O
147	SD0_CLK	SD0_CLK/GPE5	SD0 clock	O
148	SD0_DAT0	SD0_DAT0/GPE7	SD0 data	I/O
149	SD0_DAT1	SD0_DAT1/GPE8	SD0 data	I/O
150	SD0_WPn	UCLK/GPH12	External clock for UART	I/O
151	WAITn	nWAIT	Requests to prolong a current bus cycle	I
152	CSn1	nRCS1/GPA12	Chip select	O
153	CSn2	nRCS2/GPA13	Chip select	O
154	CSn3	nRCS3/GPA14	Chip select	O
155	CSn4	nRCS4/GPA15	Chip select	O
156	CSn5	nRCS5/GPA16	Chip select	O
157	CSn0	nRCS0	Chip select	O
158	NC		Option	
159	GND	Ground		P
160	GND	Ground		P
161	VDD_IO	3.3V Power in		P
162	VDD_IO	3.3V Power in		P
163	DATA8	RDATA8	Data Bus	I/O
164	DATA9	RDATA9	Data Bus	I/O
165	DATA10	RDATA10	Data Bus	I/O
166	DATA11	RDATA11	Data Bus	I/O
167	DATA12	RDATA12	Data Bus	I/O
168	DATA13	RDATA13	Data Bus	I/O
169	DATA14	RDATA14	Data Bus	I/O
170	DATA15	RDATA15	Data Bus	I/O
171	ADDR25	RADDR25	Address Bus	O
172	ADDR0	RADDR0	Address Bus	O
173	WEn	nRWE	Indicates the bus cysle is a write cycle	O
Pin	Signal name	Function	Description	IO Type
174	OEn	nROE	Indicates the bus cycle is a read cycle	O
175	ADDR20	RADDR20	Address Bus	O
176	ADDR19	RADDR19	Address Bus	O
177	ADDR18	RADDR18	Address Bus	O
178	ADDR17	RADDR17	Address Bus	O
179	ADDR16	RADDR16	Address Bus	O
180	ADDR15	RADDR15	Address Bus	O
181	ADDR14	RADDR14	Address Bus	O
182	ADDR13	RADDR13	Address Bus	O
183	ADDR12	RADDR12	Address Bus	O

184	ADDR11	RADDR11	Address Bus	O
185	ADDR10	RADDR10	Address Bus	O
186	ADDR9	RADDR9	Address Bus	O
187	DATA0	RDATA0	Data Bus	I/O
188	DATA1	RDATA1	Data Bus	I/O
189	DATA2	RDATA2	Data Bus	I/O
190	DATA3	RDATA3	Data Bus	I/O
191	DATA4	RDATA4	Data Bus	I/O
192	DATA5	RDATA5	Data Bus	I/O

1.6 OM Fast SET and NC Pin Option Circuit



◆ Pin77 (OM3): Set L is Flash Boot mode, H is SD Boot mode.



◆ If use RADDR21-24, must be modify these parts.

1.7 Multiplexed GPIO

Pin	Signal name	Function 1	Function 2	Function 3
134	TOUT3	TOUT3	GPB3	
135	TOUT2	TOUT2	GPB2	
136	TOUT1	TOUT1	GPB1	
137	TOUT0	TOUT0	GPB0	

◆ 32bit PWM timer output

Pin	Signal name	Function 1	Function 2	Function 3
75	NC	NC	RADDR21	GPA6
76	NC	NC	RADDR22	GPA7
77	OM3	OM_SET	RADDR23	GPA8
78	NC	NC	RADDR24	GPA9
171	ADDR25		RADDR25	RDATA_OEN
175	ADDR20		RADDR20	GPA5
176	ADDR19		RADDR19	GPA4
177	ADDR18		RADDR18	GPA3
178	ADDR17		RADDR17	GPA2
179	ADDR16		RADDR16	GPA1

◆ OM and Address option pins

Pin	Signal name	Function 1	Function 2	Function 3
33	RXD2	RXD2	GPH5	
34	TXD2	TXD2	GPH4	
35	RXD1	RXD1	GPH3	
36	TXD1	TXD1	GPH2	
37	RXD0	RXD0	GPH1	
38	TXD0	TXD0	GPH0	

39	RTSn0	RTSn0	GPH9	
40	CTSn0	CTSn0	GPH8	
41	RTSn1	RTSn1	GPH11	
42	CTSn1	CTSn1	GPH10	
43	RXD3	RXD3	GPH7	nCTS2
44	TXD3	TXD3	GPH6	nRTS2
150	SD0_WPn	UCLK	GPH12	

◆ UART Pins

Pin	Signal name	Function 1	Function 2	Function 3
104	I2C_SCL	I2C_SCL	GPE14	
105	I2C_SDA	I2C_SDA	GPE15	

◆ I2C Pins

Pin	Signal name	Function 1	Function 2	Function 3	Function 4
88	I2S_CDCLK	I2S_CDCLK	PCM_CDCLK	AC97_BITCLK	GPE2
89	I2S_LRCK	I2S_LRCK	PCM_FSYNC	AC97_nRESET	GPE0
90	I2S_SCLK	I2S_SCLK	PCM_SCLK	AC97_SYNC	GPE1
93	I2S_SDI	I2S_SDI	PCM_SDI	AC97_SDI	GPE3
94	I2S_SDO	I2S_SDO0	PCM_SDO	AC97_SDO	GPE4
130	GPB9	I2S_SDO1	nXDACK0		GPB9
131	GPB10	I2S_SDO2	nXDREQ0		GPB10

◆ Audio codec interface

Pin	Signal name	Function 1	Function 2	Function 3
67	SPIMISO	SPIMISO	GPE11	
68	SPICS	SPICS	GPL13	
69	SPICLK	SPICLK	GPE13	
70	SPIMOSI	SPIMOSI	GPE12	

◆ SPIs interface

Pin	Signal name	Function 1	Function 2	Function 3
73	CLKOUT1	CLKOUT1	GPH14	
142	CLKOUT0	CLKOUT0	GPH13	

◆ Clock output

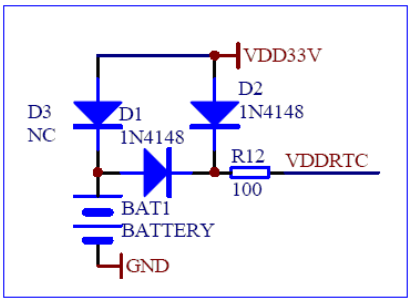
Pin	Signal name	Function 1	Function 2	Function 3
87	GPA23	L3CLK	GPA23	RSMCLK
91	GPA24	L3DATA	GPA24	RSMVAD
92	GPM0	L3MODE	GPM0	RSMBWAIT

◆ L3 control bus

Chapter 2 How to use the module

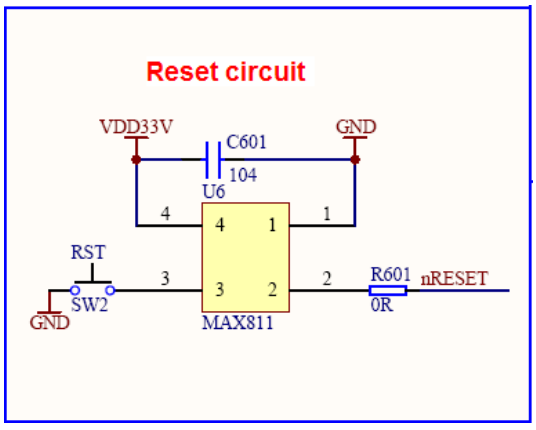
2.1 Peripheral circuit reference

2.1.1 RTC battery circuit

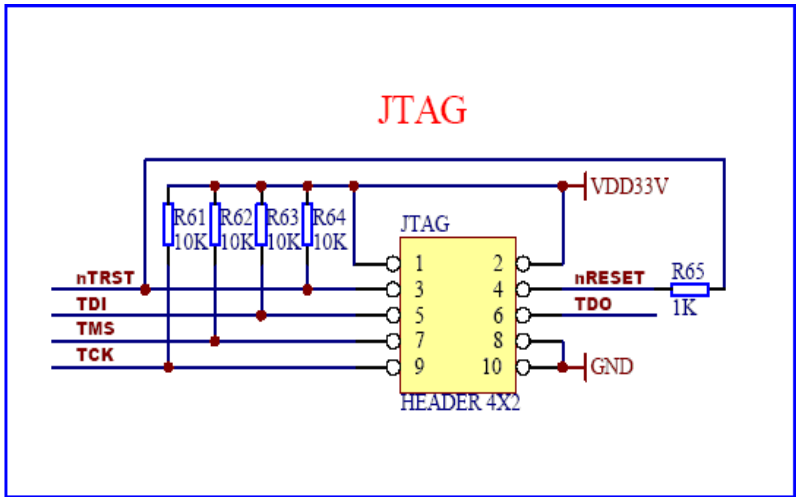


If not use, The Pin58 cannot NC.

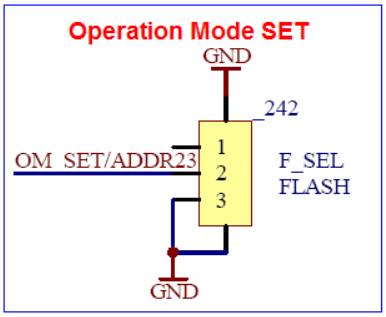
2.1.2 Reset circuit



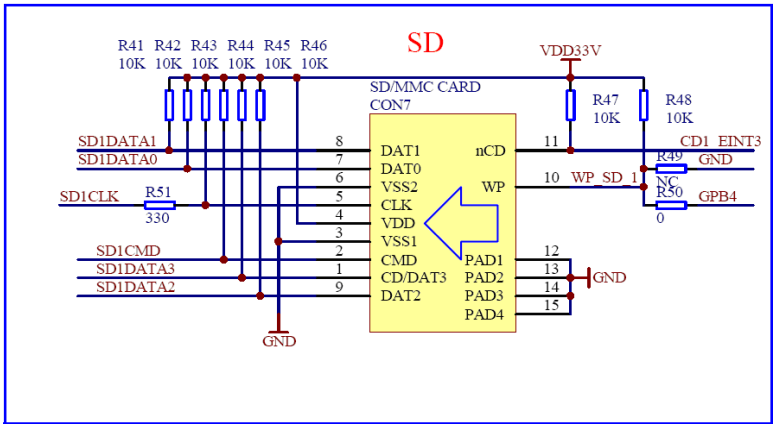
2.1.3 JATG circuit



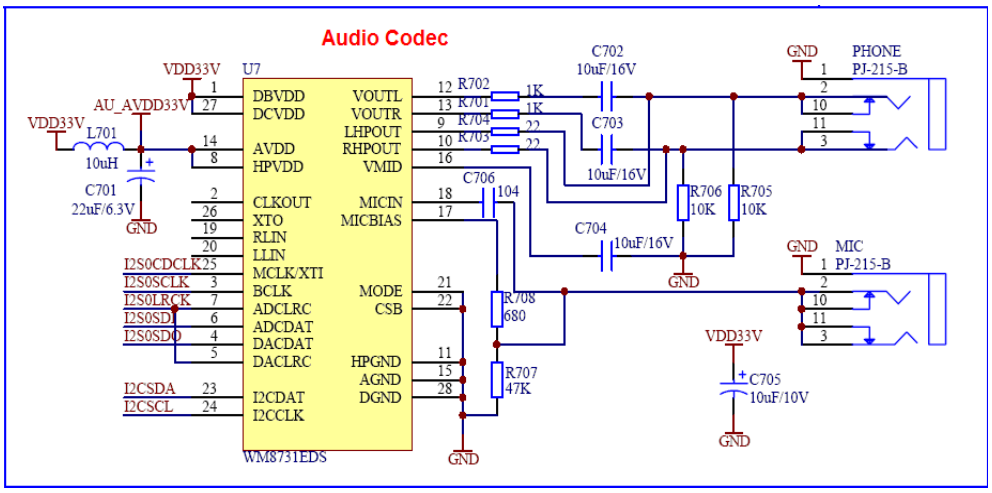
2.1.4 OM setting circuit



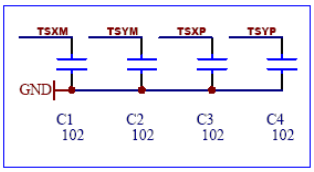
2.1.5 SD1 interface circuit



2.1.6 Audio codec circuit

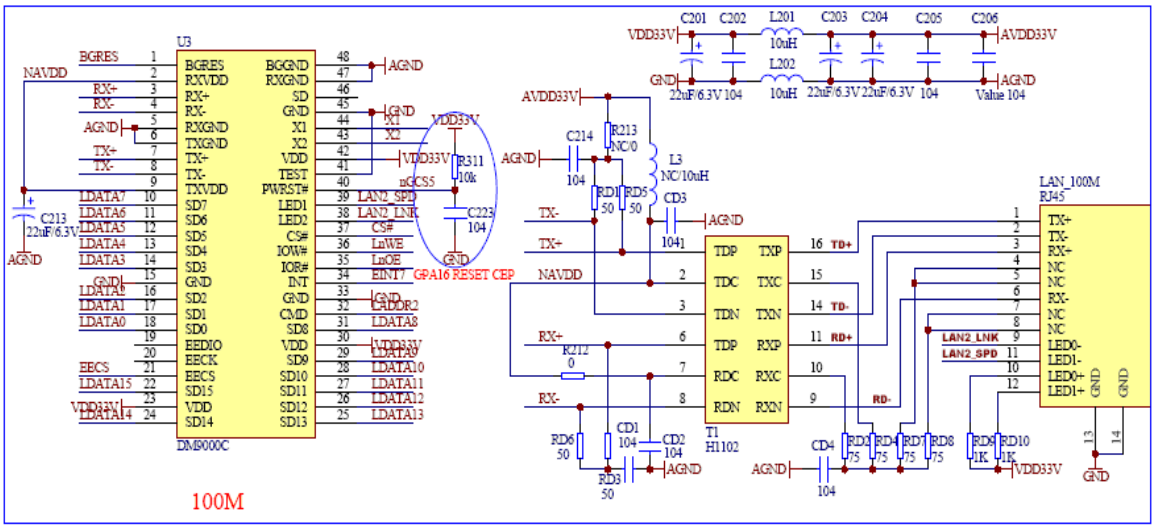


2.1.7 Res-Touch circuit

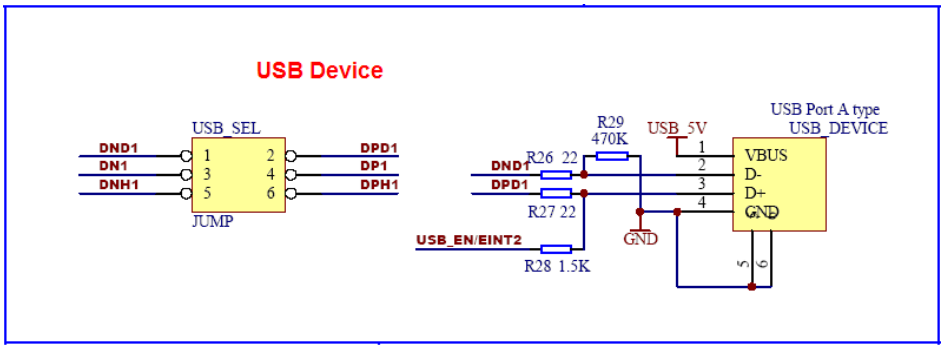


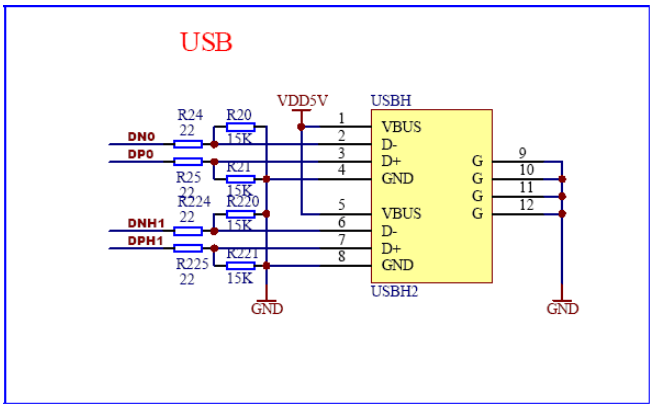
Close to CPU module.

2.1.8 Ethernet interface circuit



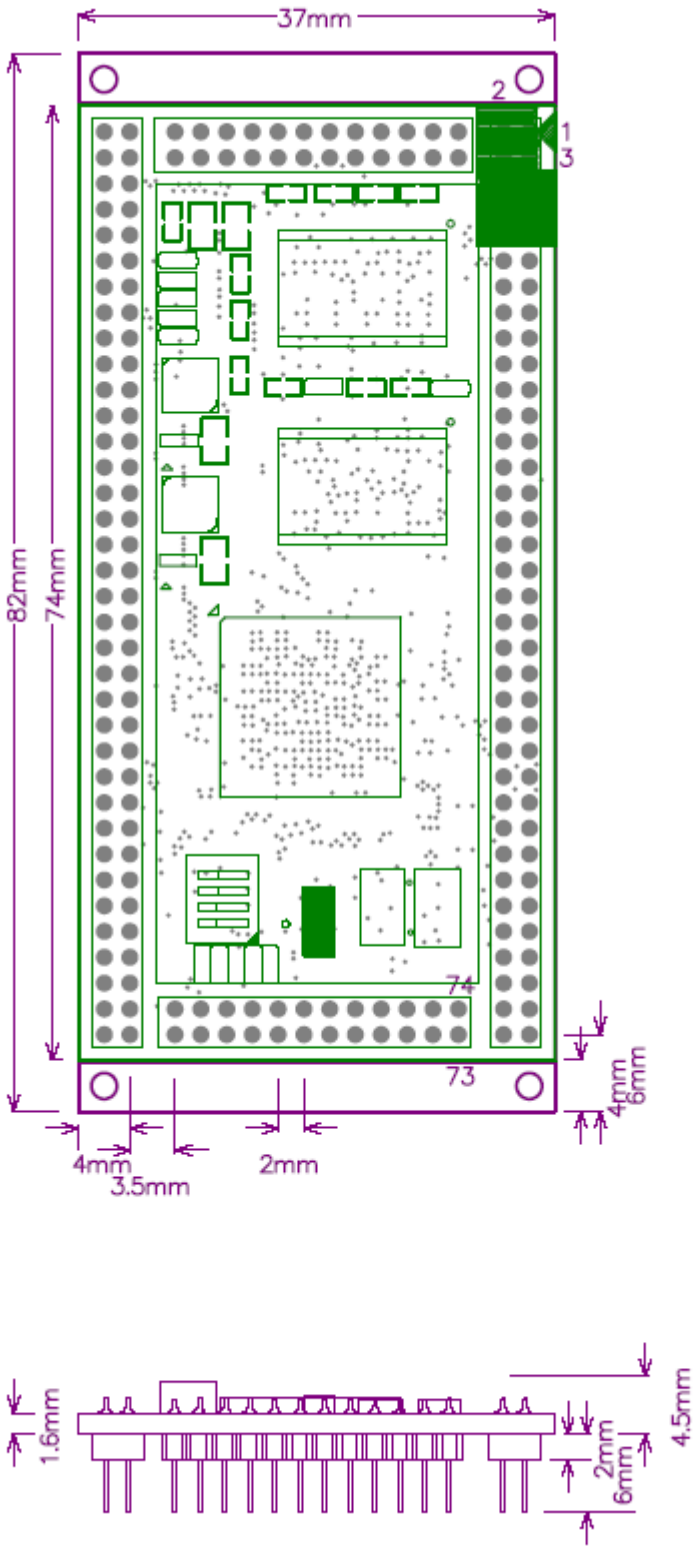
2.1.9 USB interface circuit



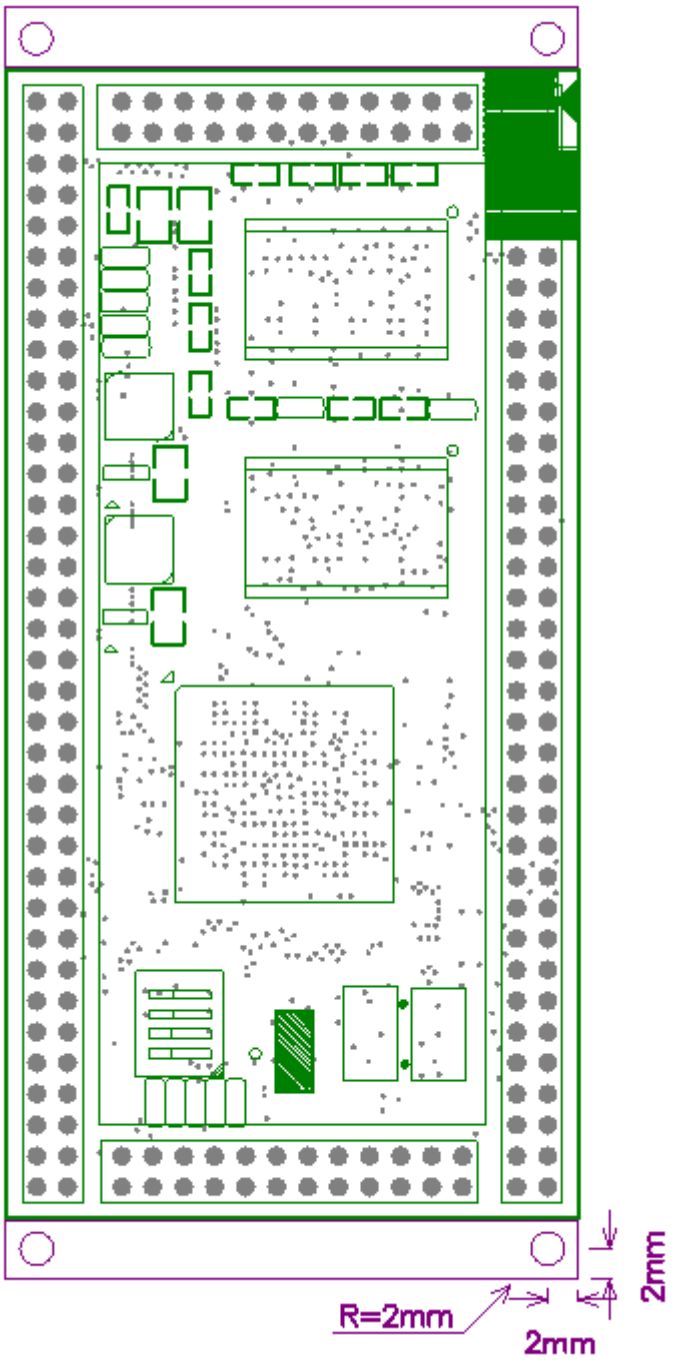


2.2 Dimensions and Footprint

2.2.1 Mechanical Specifications



2.2.2 Hole specifications



Chapter 3 Electric Property and Certifications

3.1 Electric property

3.1.1 Dissipation and Temperature

Symbol	Parameter	Min	Typ	Max	Unit
VDD_IO	IO Supply Voltage	3.3-5%	3.3	3.3+5%	V
Vrvpp	Max ripple Voltage			0.15	V
Imax	VDD_IO Max Current		165	175	mA
VCC_RTC	RTC Battery Voltage	2.5	3	3.6	V
Irtc	RTC Input Current			10	uA
Ta	Operating Temperature	0		70	℃
Tstg	Storage Temperature	-40		85	℃

3.1.2 Reliability of test

High Temperature Operating Test		
Contents	Operating 8 h in high temperature	55℃+/-2℃
Result	Pass	

Operating life Test		
Contents	Operating in room	120h
Result	Pass	

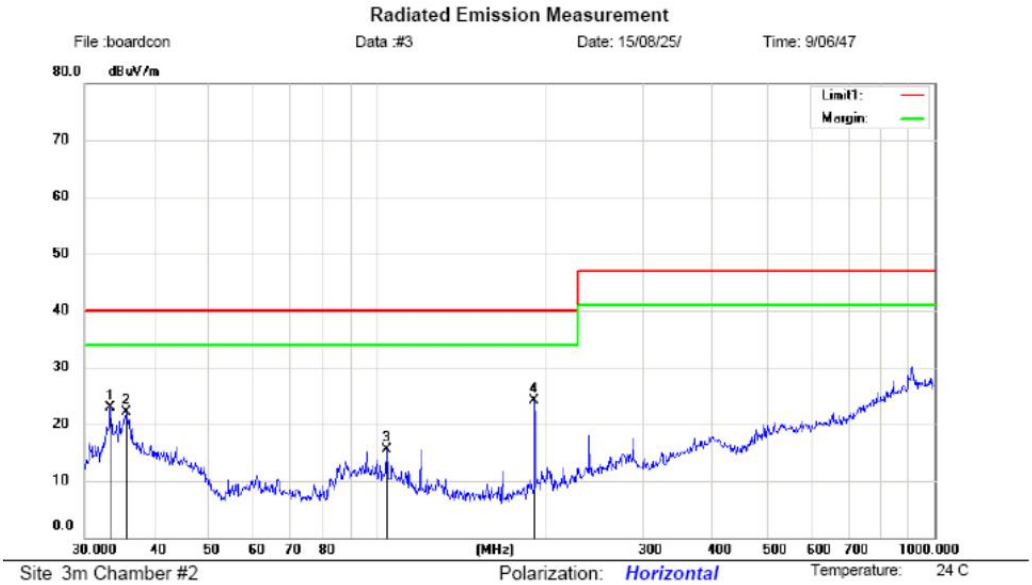
3.2 Certifications

3.2.1 Environmental testing

The module conforms to ROHS.

3.2.2 Certifications

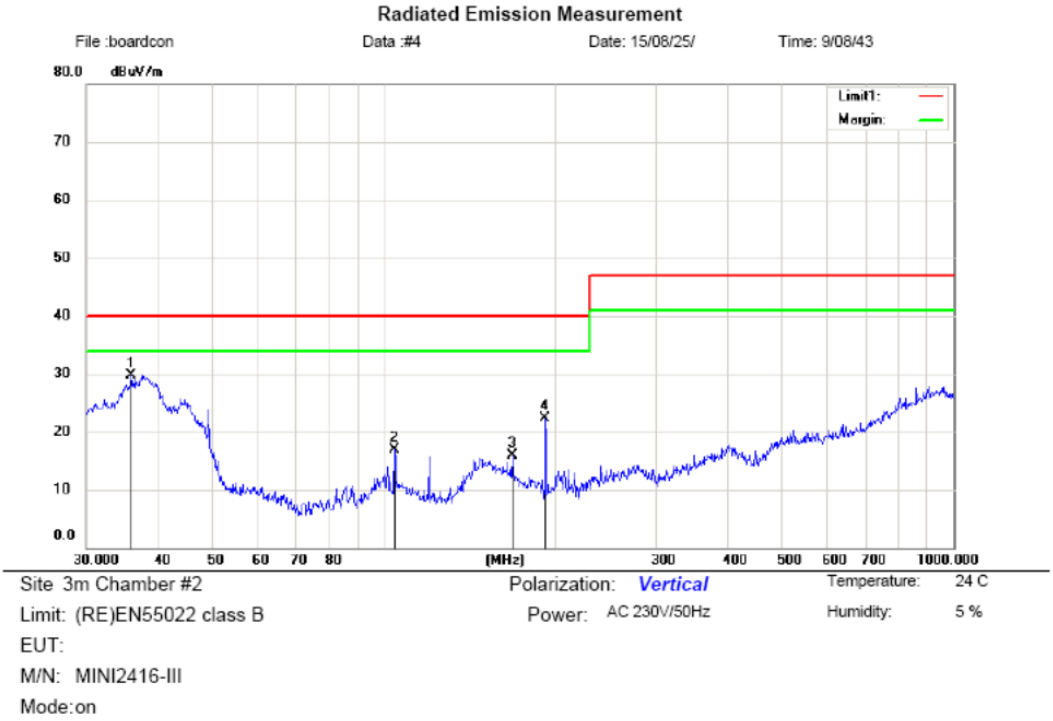
The module conforms to CE. No. **PRSZ15082501E.**



Site 3m Chamber #2
Limit: (RE)EN55022 class B
EUT:
M/N: MINI2416-III
Mode:on
Polarization: *Horizontal*
Power: AC 230V/50Hz
Temperature: 24 C
Humidity: 5 %

Note: 2#

No.	Mk.	Freq.	Reading Level	Correct Factor	Measure-ment	Limit	Over		Antenna Height	Table Degree	
		MHz	dBuV	dB	dBuV/m	dBuV/m	dB	Detector	cm	degree	Comment
1		33.3280	37.13	-14.24	22.89	40.00	-17.11	peak			
2		35.6240	35.75	-13.65	22.10	40.00	-17.90	peak			
3		104.1701	30.00	-14.43	15.57	40.00	-24.43	peak			
4	*	191.7450	41.33	-17.16	24.17	40.00	-15.83	peak			



Note: 2#

No.	Mk.	Freq.	Reading Level	Correct Factor	Measure-ment	Limit	Over		Antenna Height	Table Degree	
		MHz	dBuV	dB	dBuV/m	dBuV/m	dB	Detector	cm	degree	Comment
1	*	35.8746	43.27	-13.60	29.67	40.00	-10.33	peak			
2		104.1701	31.30	-14.43	16.87	40.00	-23.13	peak			
3		167.8243	35.10	-19.17	15.93	40.00	-24.07	peak			
4		191.7450	39.46	-17.16	22.30	40.00	-17.70	peak			